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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,175	03/02/2004	Hayden C. Cranford JR.	RPS920030105US1	3190

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EXAMINER	
LEE, SIU M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
10/18/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/791,175	CRANFORD ET AL.	
	Examiner	Art Unit	
	Siu M. Lee	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7-9 and 13-16* is/are rejected.

7)☒ Claim(s) *3-6, 10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Remarks

1. Applicant's remarks, see page 6, filed 8/1/2007, with respect to Draw Objection have been fully considered and are persuasive. The objection of the drawing has been withdrawn.

2. Applicant's arguments, see page 7, filed 8/1/2007, with respect to 35 U.S.C. §112 rejection of claims 3-6 have been fully considered and are persuasive. The 35 U.S.C. §112 rejection of claims 3-6 has been withdrawn.

3. Applicant's arguments with respect to claims 1-3, 7-8, 13-14, and 16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Makarov (US 7,075,948 B2).

(1) Regarding claim 1:

Makarov discloses a circuit comprising:

a controller (counter-clockwise transition detector 102 and the clockwise transition detector 104 in figure 5) for generating first signals for phase adjusts in a receiver link to adapt to frequency offsets (counter-clockwise transition detector 102 and the clockwise transition detector 104 in figure 5 output a first signal D (D_{ccw} for the detector 102 and D_{cw} for the detector 104) when active indicates a detected occurrence of a transition event for the received signal, column 6, lines 23-38); and

an adjust circuit (counter 108 and processing component 112 in figure 5) coupled to the controller, the adjust circuit for detecting trends in the signals (the counter 108 includes a counter-clockwise accumulator 108(1) for counting the active signals D_{ccw} over a given time period and a clockwise accumulator 108(2) for counting the active signals D_{cw} over the same given time period, by accumulating the clockwise and counter-clockwise signal over a time period, the counting value of the counters 108(1) and 108(2) detect a trend of the phase adjust in the signal), using combinatorial logic (adder 116 in figure 5) to adapt the signal based on accumulated data, and generating second signal improving a rate of compensation for the frequency offsets by the phase adjusts (the output of the counter 108 at the expiration of each time period is a count N (N_{ccw} for the counter clockwise accumulator 108(1) and N_{cw} for the clockwise accumulator 108(2)) that represent the sum number of occurrence of a detected transition event in each direction for the received signal during the given time period, adder 116 subtract the count Ncw of the clockwise accumulator 108(2) from the count Nccw of the counter clockwise accumulator 108(1) and output the second signal, the

processing components (sign portion 118 and processing component 122 in figure 5) examine the sign and the value portion of the second signal and use the sign and magnitude value of the second signal directly for frequency offset correction and thus improve a rate of compensation for the frequency offset, column 6, line 39 – column 7, line 3).

(2) Regarding claim 2:

Makarov discloses wherein the first signal comprises a first rotate up and a first rotate down signal (counter clockwise signal (D_{ccw}) and the clockwise signal (D_{cw}) from the CCW detector 102 and CW detector 104 in figure 5) and the second rotate up and a second rotate down signal (the N_{ccw} signal from the counter clockwise signal accumulator 108(1) and the N_{cw} signal from the clockwise signal accumulator 108(2) as shown in figure 5).

6. Claims 9, 15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Usui (US 6,615,060 B1).

(1) Regarding claim 9:

Usui discloses a circuit comprising:

an up/down counter (up/down counter 142 in figure 3) for counting signals for phase adjustments by a clock-data-recovery loop of a serial receiver (cell phone receiver as disclose in figure 1 receives signal serially) (the up/down counter 142 in figure 3 receives the advance/delay signal 146 from the advance/delay detecting unit 141 and up/down counter 142 carries out addition or subtraction at timing of the

demodulation clock signal in response to the advance/delay signal 146, column 6, lines 37-39), wherein the signals comprise rotate up and rotate down signals(advance/delay detecting unit 141 determines the phase difference between the first half of a symbol period and the second half of the symbol period at timing of the data clock signal 131 and supplies the phase difference to a up/down counter 142 as an advance/delay signal 146, column 6, lines 22-27, to correct a phase by an advance or delay signal is the same as a rotate up and rotate down signal to adjust the phase);

an adder (adder 144 in figure 3) coupled to the up/down counter (adder 144 is couple to the up/down counter 142 as shown in figure 3) that outputs accumulated data indicative of a trend in the phase adjustments (as the up/down counter is accumulating the up and down signal output by the advance/delay detecting unit for a period of time, the output of the counter 142 is an indicative of the trend in the phase adjustment over that period of time); and

combinatorial logic (phase correcting 123 in figure 2) coupled to the adder to adapt the rotate up and rotate down signals based on the accumulated data (the phase correcting unit 123 is coupe to the adder 144 in the clock reproducing unit 124 and responsive to the phase data signal and performs phase correction of the received phase data signal 129, column 5, lines 50-52).

(2) Regarding claim 15:

Usui discloses a method comprising:

monitoring trends of phase adjusts of a clock-data-recovery circuit (advance/delay signal 146 in figure 3) to a reference clock (the switch 145 transmit the

demodulation clock signal 133 to the up/down counter 142, column 6, lines 31-32) of a serial receiver (cell phone receiver as disclose in figure 1 receives signal serially) including utilizing an up-down counter (up/down counter 142 in figure 3) and an adder (adder 144 in figure 3) to accumulate phase adjust data from the phase adjusts (the up/down counter 142 accumulate the advance/delay signal 146 from the advance/delay detecting unit 141, column 6, lines 37-39), and;

adapting the phase adjusts to create future adjusts based on previous adjusts including utilizing combinatorial logic (adder 144 in figure 3) to generate the future adjust based on the accumulated phase adjust data and the previous adjusts (an advance an advance/delay detecting unit 141 determines the phase difference and supplies the phase difference to a up/down counter 142 as an advance/delay signal 146, up/down counter 142 carries out addition or subtraction at timing of the demodulation clock signal in response to the advance/delay signal 146, adder 144 adds an output value from the counter 143 and an output value from the up/down counter 142, and produces an output signal of seven bits, column 6, lines 20-48).

(3) Regarding claim 16:

Usui discloses wherein the phase adjusts further comprise rotate up and rotate down signals (advance/delay signal 146 in figure 3) for phase rotation in the clock recovery circuit.

7. Claims 7, 8, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Usui (US 6,269,128 B1).

(1) Regarding claim 7:

Usui discloses circuit (figure 2) comprising:

a up/down counter (up/down counter 211 in figure 2) for counting signals from a phase rotator control (lead/lag detector 210) for phase adjustments by a clock-data-recovery loop of a serial receiver (the clock recovery control is being used in a receiver that receives signal serially) (the up/down counter 211 increments or decrements a counter with each reference clock depending on the up/down signal UD and the up/down enable signal UDEN from the lead/lag detector 210 in figure 2, column 5, lines 9-11); and

an adder (adder 213 in figure 2) coupled to the up/down counter (adder 213 is coupled to the up/down counter 211) that outputs accumulated data indicative of a trend in the phase adjustments (the respective output counters of the up/down counter 211 and the self running up counter 212 are added by the full adder 213 to produce the symbol clock CLK, column 5, lines 44-46, as the up/down counter is accumulating the up and down signal output by the lead/lag detector 210 for a period of time, the output of the adder 213 is an indicative of the trend in the phase adjustment over that period of time).

(2) Regarding claim 8:

Usui further discloses that the signals comprise rotate up and rotate down signals (the lead/lag detector 210 determines whether the phase signal S_{PH} leads or lags behind the corresponding ideal phase, when leading, the lead/lag detector 210 sets an up/down signal UD to "1" and an up/down enable signal UDEN to "1" and, when lagging,

the up/down signal UD to "0" and the up/down enable signal UDEN to "1", column 4, lines 58-63, the up/down counter 211 increments or decrements a counter with each reference clock depending on the up/down signal UD and the up/down enable signal UDEN).

(3) Regarding claim 13:

Usui discloses a method comprising:

monitoring trends of phase adjusts of signals from a phase rotator control (the lead/lag detector 210 in figure 5) of a clock-data-recovery circuit to a reference clock (reference clock f_{REF} in figure 5) of a serial receiver (the clock recovery control is being used in a receiver that receives signal serially) (the up/down counter 211 in figure 2 monitor the up/down signal (UD) and up/down enable signal (UDEN) output from the lead/lag detector 210 for a period of time, the up/down counter 211 increments or decrements a counter with each reference clock, column 4, line 66 – column 5, lines 11, as the up/down counter is accumulating the up and down signal output by the lead/lag detector 210 for a period of time, the output of the adder 213 is an indicative of the trend in the phase adjustment over that period of time); and

adapting the phase adjusts to create future adjusts based on previous adjusts (the output of the lead/lag detector 210 (UD and UDEN) is accumulate in the up/down counter 211 for a period of time and the up/down counter output to the full adder 213 to produce the symbol clock CLK, column 5, lines 44-46, as the up/down counter is accumulating the output of the lead/lag detector, it is accumulating previous adjust for a future adjust).

(4) Regarding claim 14:

Usui further discloses that the step of monitoring comprises utilizing an up-down counter (up/down counter 211 in figure 2) and an adder (adder 213 in figure 2) to accumulate phase adjust data from the phase adjust (adder 213 is adding the accumulated phase adjust from the up/down counter 211, column 5, lines 44-46).

Allowable Subject Matter

8. Claims 3-6 and 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

The present invention describes a circuit and method for providing automatic adaptation to frequency offsets in high speed serial links. The closest prior art (Makarov (US 7,075,948 B2), Usui (US 6,269,128 b1) and Usui (6,615,060 B1)) disclose a similar system but fail to describe a circuit wherein the adjust circuit monitors for an overflow or underflow of the first rotate up and rotate down signal and the adder accumulates a chosen number of most significant bits of the rotate up and rotate down signals. These distinct features have been added to the dependent claim 3-6 and 10-12, thus rendering them allowable.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Schmatz et al. (US 2004/0208170 A1) discloses a clock data recovering system with external early/late input.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M Lee
Examiner
Art Unit 2611
10/2/2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER